JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY KAKINADA
KAKINADA – 533 003, Andhra Pradesh, India
DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

III Year – II Semester		L	T	P	C
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VLSI DESIGN					

UNIT-I:
INTRODUCTIONANDBASICELECTRICALPROPERTIESOFMOSCIRCUITS:
VLSI Design Flow, Introduction to IC technology, Fabrication process: nMOS, pMOS and CMOS. I_{ds} versus V_{ds} Relationships, Aspects of MOS transistor Threshold Voltage, MOS transistor Trans, Output Conductance and Figure of Merit. nMOS Inverter, Pull-up to Pull-down Ratio for nMOS inverter driven by another nMOS inverter, and through one or more pass transistors. Alternative forms of pull-up, The CMOS Inverter, Latch-up in CMOS circuits, Bi-CMOS Inverter, Comparison between CMOS and BiCMOS technology, MOS Layers, Stick Diagrams, Design Rules and Layout, Layout Diagrams for MOS circuits

UNIT-II:
BASIC CIRCUIT CONCEPTS: Sheet Resistance, Sheet Resistance concept applied to MOS transistors and Inverters, Area Capacitance of Layers, Standard unit of capacitance, some area Capacitance Calculations, The Delay Unit, Inverter Delays, driving large capacitive loads, Propagation Delays, Wiring Capacitances, Choice of layers.
SCALING OF MOS CIRCUITS: Scaling models and scaling factors, Scaling factors for device parameters, Limitations of scaling, Limits due to sub threshold currents, Limits on logic levels and supply voltage due to noise and current density. Switch logic, Gate logic.

UNIT-III:
BASIC BUILDING BLOCKS OF ANALOG IC DESIGN: Regions of operation of MOSFET, Modelling of transistor, body bias effect, biasing styles, single stage amplifier with resistive load, single stage amplifier with diode connected load, Common Source amplifier, Common Drain amplifier, Common Gate amplifier, current sources and sinks.

UNIT-IV:
CMOS COMBINATIONAL AND SEQUENTIAL LOGIC CIRCUIT DESIGN:
Static CMOS Design: Complementary CMOS, Rationed Logic, Pass-Transistor Logic.
Dynamic CMOS Design: Dynamic Logic-Basic Principles, Speed and Power Dissipation of Dynamic Logic, Issues in Dynamic Design, Cascading Dynamic Gates, Choosing a Logic Style, Gate Design in the Ultra Deep-Submicron Era, Latch Versus Register, Latch based design, timing decimation, positive feedback, in stability, Meta stability, multiplexer based latches, Master-Slave Based Edge Triggered Register, clock to q delay, setup time, hold time, reduced clock load master slave registers, Clocked CMOS register. Cross coupled NAND and NOR, SR Master Slave register, Storage mechanism, pipelining.

UNIT-V:
FPGA DESIGN: FPGA design flow, Basic FPGA architecture, FPGA Technologies, Introduction to FPGA Families.
INTRODUCTIONTOADVANCEDTECHNOLOGIES: Giga-scale dilemma, Short channel effects, High–k, Metal Gate Technology, Fin-FET, TFET.

TEXTBOOKS:

1. Essentials of VLSI Circuits and Systems – Kamran Eshraghian, Douglas and A.Pucknell and Sholeh Eshraghian, Prentice-Hall of India Private Limited, 2005 Edition.
2. Design of Analog CMOS Integrated Circuits by Behzad Razavi, McGraw Hill, 2003
3. Digital Integrated Circuits, Jan M.Rabaey, Anantha Chandrakasan and Borivoje Nikolic, 2nd edition, 2016.

REFERENCES:

1. "Introduction to VLSI Circuits and Systems", John P.Uyemura, John Wiley&Sons, reprint 2009.
2. Integrated Nano electronics: Nano scale CMOS, Post-CMOS and Allied Nano technologies Vinod Kumar Khanna, Springer India, 1stedition, 2016.
3. Fin-FETs and other multi-gate transistors, Colinge JP, Editor NewYork, Springer, 2008.

Course Outcomes:

At the end of this course the student will be able to:

1. Demonstrate a clear understanding of CMOS fabrication flow and technology scaling.
2. Apply the design Rules and draw layout of a given logic circuit.
3. Design basic building blocks in Analog IC design.
4. Analyze the behavior of amplifier circuits with various loads.
5. Design various CMOS logic circuits for design of Combinational logic circuits.
6. Design MOSFET based logic circuits using various logic styles like static and dynamic CMOS.
7. Design various applications using FPGA.